PROCESS FOR FABRICATING SEMICONDUCTOR DEVICE

This is a CIP application of U.S.S.N. 09/026,097 filed on February 19, 1998, now abandoned

BACKGROUND OF THE INVENTION

The present invention relates to processes for fabricating semiconductor devices and, more particularly, to a semiconductor fabrication process in which a buried layer is formed.

In semiconductor devices such as semiconductor integrated circuits, a p^+ buried layer is provided for the application of an "up-down isolation" technique. In up-down isolation, an region is not only diffused downwardly from the surface of an epitaxial layer but also is rediffused upwardly from below the epitaxial layer, i.e., from the substrate side. With this technique, the diffusion time is shortened so as to suppress the lateral spread of the isolation (p-diffusion). Accordingly, the chip area can be reduced and, at the same time, the breakdown voltage of the completed semiconductor device is increased because of limited upward diffusion of the n^+ region.

Taking an npn transistor as an example of a semiconductor device having a buried layer, a first related process sequence for forming the buried layer in this transistor is described hereinafter with reference to Figs. 1 through 4. In step 1 shown in Fig. 1, a p-type substrate 11 typically made of silicon is provided with an oxide film mask 12, such as an SiO_2 film, arranged so that the surface of the